CMOS ISFET-BASED STRUCTURES FOR BIOMEDICAL APPLICATIONS

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Abstract **– The miniaturization and integration of biomedical sensors is of key importance for improved diagnosis and therapy in the future. These devices integrated monolithically on the same chip together with low-power electronics are suitable for implantable "in vivo" monitoring of arterial blood pH, pCO_2 or pO_2 changes.**

This paper deals with the design, fabrication and experimental evaluation of ISFET-based structures realized in an unmodified commercial submicron 0.6µm CMOS technology. The compatibility study of pH ISFET chemical devices with CMOS circuits is described. Some technology-driven problems associated with using this submicron process for the chemical microsensors are reported. Comparison of our fabricated structures with previously published ISFETs using unmodified standard CMOS technology is given. Research goals are to develop fully integrated CMOS compatible ion-sensitive ISFET devices for implantable biomedical microsystems.

I. INTRODUCTION

The ion-sensitive chemical sensor (ISFET) is based on MOSFET device structure thus, it can be manufactured using a CMOS process, the most interesting technology for microsystems [1]. A schematic cross section of N/P type ISFETs is shown in Fig. 1. Devices are usually fabricated on a p-Si substrate. The ISFET gate area can consist of one or several dielectric layers.

The original gate material used was SiO_2 [2]. The pH-sensing properties and drift behavior of the ISFET improved greatly with the introduction of other insulating materials. Commonly used pH-sensitive membranes on top of the gate area are Si_3N_4 [3], Al_2O_3 [3, 4] or Ta_2O_5 [3, 5], because of the higher pH sensitivity, selectivity, and long-term stability.

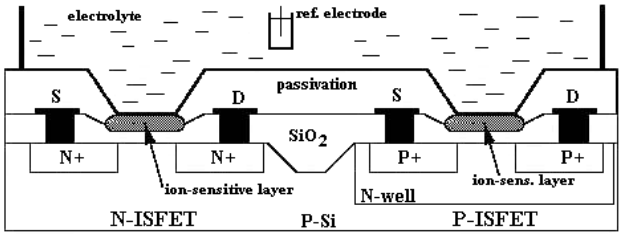

Fig. 1. Schematic cross section of N and P-type ISFETs in CMOS technology.

Unfortunately, technological steps usually employed for making mentioned ISFET gate membranes are not compatible with standard CMOS processes, which use polysilicon gate to define self-aligned source and drain transistor regions.

Several authors published different methods of fabricating ISFETs on the basis of a modified standard CMOS process [1, 6-8] with additional process steps. References [6, 7] propose that the ISFETs be designed with a standard polysilicon gate for self-alignment of the source and drain regions. Reference [6] proposed leaving the polysilicon on the ISFET as a floating gate, while another [7] proposed the removal of the polysilicon gate by etching. Disadvantages of these two methods are the necessary modifications to the standard CMOS process, namely the use of tungsten silicide as the metallisation layer [6] and a very delicate etching of the polysilicon gate [7].

A customized 2.5µm CMOS technology (double poly, single metal layer) was presented in [1] for the fabrication of ISFETs together with on-chip sensor circuits using three additional process steps. Another extended 1.2µm CMOS process (also double poly, single metal layer) has been described in [8] by applying four additional steps for the ISFET. These extra steps defined the ISFET gate oxide region, formation of the gate oxide and pH sensitive insulator layers, and the formation of a window in the passivation layer to expose the ISFET sensor. However, it is desirable when fabricating integrated sensors to use standard unmodified and cost-effective CMOS processes. Each non-standard process step increases the price of the device.

The research goals are to implement ISFET sensors monolithically on the same chip together with their interfacing electronics. A full ISFET fabrication compatibility with CMOS circuits can be possible due to the fact that the standard CMOS process dispose of some ion-sensitive ISFET-gate layers (SiO_2, Si_3N_4, or SiO_xN_y oxynitride passivation layer).

When a standard CMOS process will be used to fabricate an ISFET, the polysilicon layer must be left in the gate area for good source and drain area definition. This will not counteract the ISFET operation if an insulating pH-sensitive layer is on top of the polysilicon gate [9]. Several ISFET structures have been designed and characterized in [1, 9], using a commercial 1.0µm CMOS IC technology (1 polySi, 2 metal layers) without any modification or post-processing.

Sub-micron technologies are now more and more

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attractive for analog/mixed IC design, as well as for integrated microsensors development. This paper describes our research, aimed at extending the concept of realizing integrated ISFET structures to an unmodified commercial 0.6μm submicron CMOS technology (2 poly, and 3 metal layers). Ion sensitive layers are those normally available in the standard fabrication process. Several NMOS and PMOS-type ISFET structures were designed, fabricated, and tested. The ISFET devices have a gate structure compatible with the CMOS process, with a floating electrode consisting on polysilicon and several metal layers. The passivation oxynitride layer acts as the pH-sensitive material. Measurement results are discussed. Leakage current problems associated to this submicron process will be reported. A comparison of our fabricated structures with previously published ISFET devices in unmodified process is given.

II. DESIGN AND FABRICATION

The 0.6μm commercial unmodified CMOS technology has been used with following process levels: gate oxide thickness of 12.5nm, polySi of 250nm, metal 1 layer of 720nm, metal 2 of 650nm, metal 3 thickness of 940nm, and finally the passivation layer of 750nm.

The source and drain regions of ISFETs are defined by self-aligned ion implantations using the polySi gate as a mask. The oxynitride passivation has been used as the pH-sensitive layer in contact with the liquid solution. However, it is not possible to obtain a direct opening window between the gate and passivation in the standard CMOS process, so some design rule violations has been applied to design ISFET structures, as shown on the process mask flow in Fig.2. Violations of contact, via and via2 openings have been carried out.

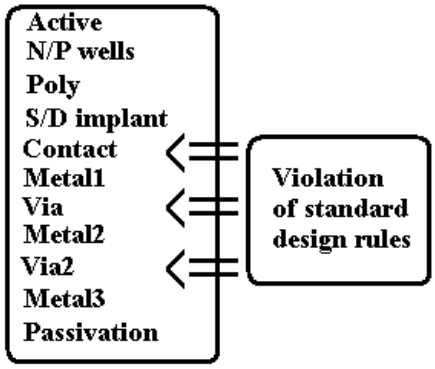

Fig. 2. Graphical representation of the CMOS process mask flow with required design rule violations for ISFET sensor designs.

Several types of ISFET structures with multi-layered gates have been designed, as shown in Fig.3. The size of the active region of the sensors has been fixed to W/L=250/30 μm. Samples A and C uses only thin gate oxide tox, the floating polysilicon gate, and the passivation layer as a sensitive membrane. Samples B and D use all conducting layers between the polysilicon gate and the nitride passivation. Accessible metal connections to the B and D gates have been added in order to compare their behaviors. Using this approach, Vgs voltage can either be applied directly of the gate or via the reference electrode immersed in a pH solution.

The design of PMOS-type ISFETs was implemented for two reasons:

1) Comparison of P-type structures with N-type ISFETs to see the pH sensitivity differences;
2) Threshold voltage Vth of P-type ISFETs (C and D) is expected to be negative, which is interesting in applications using a grounded reference electrode in a read-out circuit.

Finally, NMOS and PMOS transistors of the same dimensions have been added on the chip to compare electrical parameters of individual ISFETs with the MOSFET behaviors. An on-chip diode is used as a temperature sensor of a pH solution.

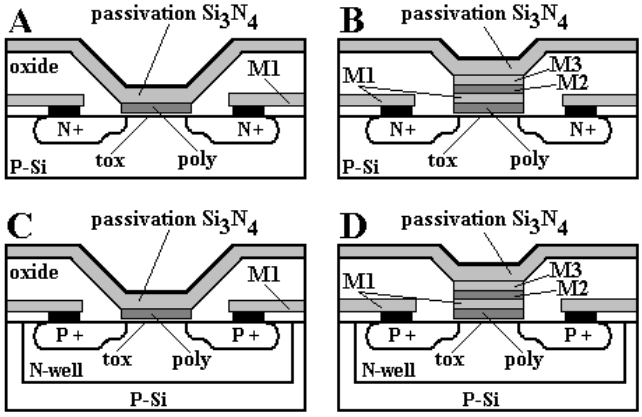

Fig. 3. Cross sections of the ISFET gate structures implemented in the submicron CMOS technology (M1=metal1, M2=metal2, M3=metal3 layers); not in scale.

Threshold voltages Vth in the range from +3.5 to +6.4V of N-type ISFET structures (similar to B sample in Fig.3) were published in 1.0μm unmodified CMOS process [1, 9]. It is higher than for NMOS devices. We also expect the Vth to be at higher positive values for B device.

Layout of the sensor chip with different experimental ISFET structures is shown in Fig.4. The total area of the chip is 3x2.5mm. A detail photo of N and P-type devices is presented in Fig.5.

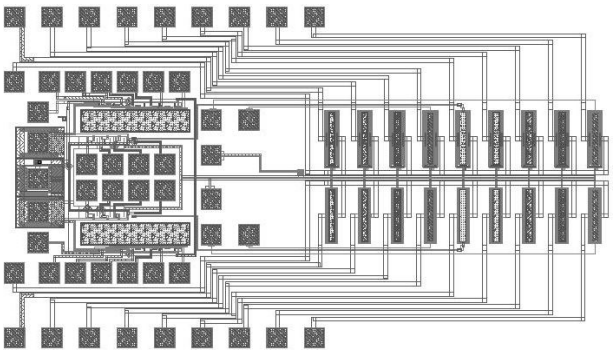

Fig. 4. Layout of the CMOS ISFET experimental structures.

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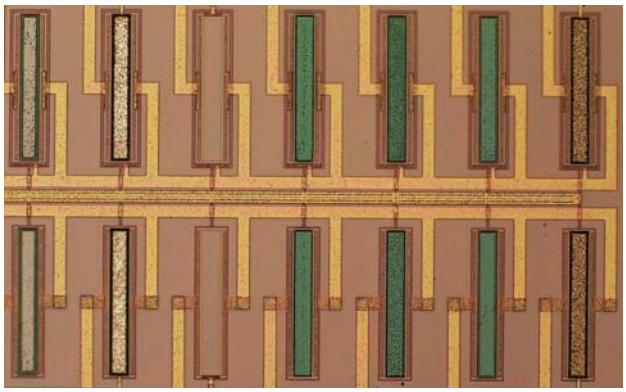


Fig. 5. Detail photo of some N and P-type ISFET microsensors, the gate area of each device is 250/30μm.

III. ENCAPSULATION AND MEASUREMENTS

Sensors were manually packaged on sticks of printed circuit boards (PCB), see Fig.6, and protected by an epoxy resin (HYSOL). This encapsulant has been tested during long time in our laboratory and demonstrated good reliability and stability (nonhydrated) in solutions from pH4 to pH10 during a month. The epoxy curing was carried out in two steps: first 2hrs @125^{o}C and then 4hrs @150^{o}C.

After encapsulation the sensors were tested for leakage currents. Three pH puffers (4.01, 7.00, 10.01) and Ag/AgCl standard liquid junction reference electrode have been used for measurements in darkness. An automated data acquisition system was applied to collect and store all the measured curves. The ISFETs were briefly etched in 1% HF solution to eliminate any surface oxide. Microsensors were kept hydrated in water, and measurements with different pH solutions have been performed each 24hours. The Ids/Vgs curves of the fabricated devices were repeated many times during 30 minutes (considered stabilization time) at each pH solution. Only steady state data were considered.

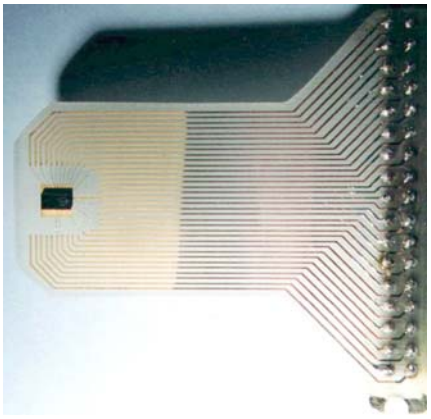


Fig. 6. PCB test probe for ISFET sensor chips before encapsulation.

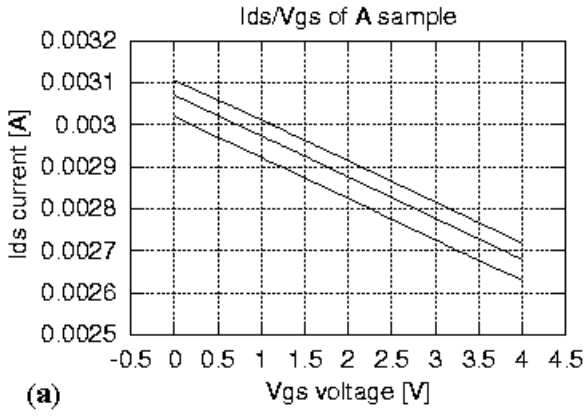
IV. RESULTS AND DISCUSSION

Three Ids/Vgs curves of A devices are shown in Fig. 7(a). Considerably high Ids current of about 3mA was measured in all A devices (Vds=5V). The current decreased linearly with Vgs applied on the reference electrode. This is an inverse-like behavior that an NMOS transistor should have. Normally, the Ids current of an NMOS transistor increases with more positive values Vgs values. No pH sensitivity was observed.

In Fig. 7(b), Ids/Vgs transfer characteristics of C structures are present. The Ids current nonlinearly decreases when Vgs becomes more positive. Relatively small Ids level of C compared with A samples can be seen. Also these structures have not resulted in operative ISFET devices.

Structures A and C have demonstrated fabrication problems. An explanation can be found in [1] for these devices: the polysilicon gate and oxide are etched away during the elimination of all metal layers from the top of the structure. Previously reported similar devices [1] did not work too.

Fabricated B devices have shown initial average sensitivity of 25mV/pH at room temperature. The sensitivity is much lower than presented by previous authors [1, 9]. The quality of sensing passivation layers differs from technology to another. Since we don't use the same CMOS process neither the same manufacturer, it is obvious that the same sensitivity cannot be expected. Measured results are shown in Fig. 8(a). The threshold voltages of B multilayered gate structures have been calculated to be about 8.5V±1V, as was expected before. However, the sensitivity has not been stable and repeatable over long period of time. After two days hydrated, Ids/Vgs characteristics considerably decreased.



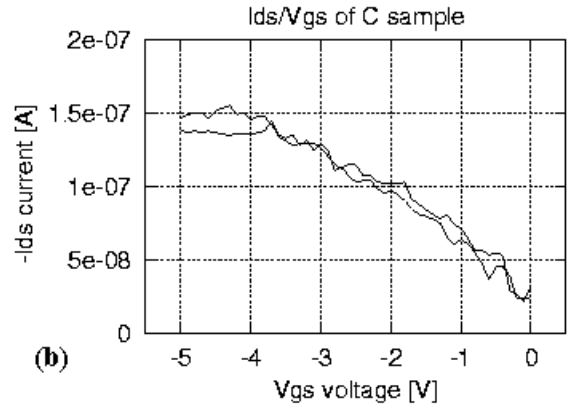


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Fig. 7. Ids versus Vgs voltage of A (a) and C (b) devices. Vgs is applied on the Ag/AgCl reference electrode, Vds=5V (-5V for C device), at room temperature.

A comparison of Ids/Vgs transfer characteristics of NMOS and B device polarized with its metal gate is shown in Fig. 8(b). We see that the characteristics are mostly equal, so the multilayered (M1+M2+M3) metal sandwich structure on top of the gate did not influence the Vth value of the N-type ISFET device.

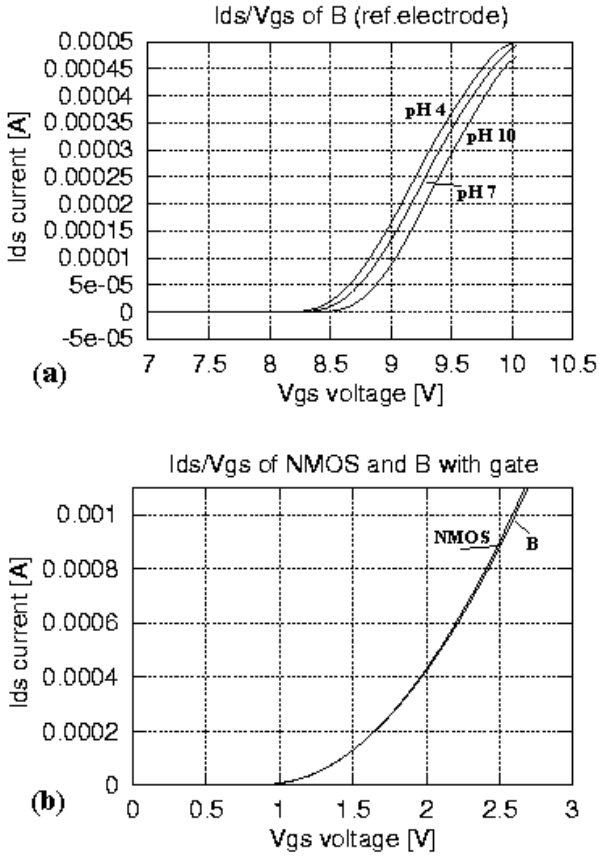

Fig. 8. Igs/Vgs characteristics of B sample with the Ag/Cl reference electrode with floating Al gate (a), and Ids/Vgs comparison between the same sized NMOS and B sensor when a same Vgs is applied on its Al gate (b), Vds=5V in both curves, at room temperature.

Very unstable characteristics were measured with D structures. Since the Id/Vgs curves changed each time and the time response and stability were not guaranteed, we were not able to measure pH sensitivity and compare it with the B structure. Only the Ids/Vgs transfer characteristics comparison of PMOS and D device polarized with its metal gate is shown in Fig. 9. The Vth of D structure decreased of about +75mV than the Vth of the same sized PMOS. Thus, P-type structure is more sensitive to the same design rules violations than the N-type. Both types of transistors have the same dimensions and openings.

Technological constraints have been found during the encapsulation and measurements. The applied 0.6μm CMOS technology is mainly used for integrated circuits, and not specially for sensors to be immersed in a liquid media. There was a problem with leakage substrate currents in some fabricated chips. The epoxy resin covers the chip, only the area close to the sensors is uncovered and is exposed to the liquid. Nevertheless, a leakage current flowing from the reference electrode to the unprotected chip substrate through microholes in the passivation layer has been measured. The oxynitride layer of this technology (750nm) seems to have a rough surface with microruptures even towards the grounded conductive p-Si substrate. Thus, the important attention had to be paid for the good encapsulation. The encapsulation procedure was applied several times and only good chips without leakage currents have been used for the measurements.

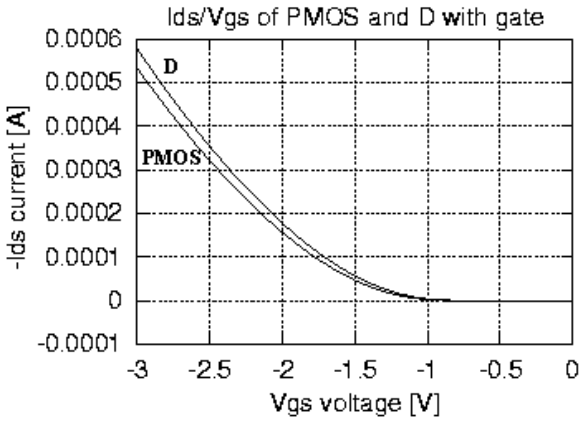

Fig. 9. Ids/Vgs comparison of D structure and the same sized PMOS with Vgs applied on their gates, Vds=-5V, at room temperature.

V. CONCLUSION AND FUTURE WORK

The design, fabrication and experimental evaluation of ISFET-based structures realized in an unmodified commercial 0.6μm CMOS technology were presented in this paper. The compatibility study of pH ISFET chemical devices with CMOS circuits was discussed. One of four designed devices has demonstrated the sensitivity of 25mV/pH with an oxynitride passivation dielectric layer as a sensitive membrane. Problems with leakage currents when using the submicron technology for chemical microsensors development were highlighted. Comparison of the fabricated structures with previously published ISFETs with unmodified CMOS process was given.

TCAD tools can be applied and each technological process step simulated in order to predict the behavior of the designed structure. Further research is needed and an exploration of inter-metal dielectric layers as pH-sensitive membrane of the technology will follow. Our effort is to try and develop fully integrated CMOS compatible ion-sensitive ISFET devices for biomedical microsystems without using additional post-process steps or technology modifications.

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